Amendments to the Drawings:

Please add Figure 6 to the drawings. A copy of Figure 6 is included in the Appendix following page 15 of this paper.

REMARKS

In the Office Action of February 23, 2006, the Examiner (1) objected to the drawings; (2) objected to the specification; (3) objected to claims 1-8 and 19-20; 4) rejected claims 1-8 and 19-20 under 35 U.S.C. § 112; 5) rejected claims 1-3, 6-7, 11-13, 16, and 18-20 under 35 U.S.C. § 102 as being anticipated by U.S. Patent No. 6,041,399 ("Terada"); 6) rejected claims 4-5, 7-9, 14-15 and 17 under 35 U.S.C. § 103 as being unpatentable over Terada in view of U.S. Patent No. 5,659,722 ("Blaner"); 7) rejected claim 10 under 35 U.S.C. § 103 as being unpatentable over Terada in view of Blaner and U.S. Patent No. 5,504,903 ("Chen").

In this Response, Applicants amend claims 1, 3, 9 and 11. Based on the amendments and arguments presented herein, Applicants respectfully request reconsideration and allowance of the pending claims.

OBJECTIONS TO THE DRAWINGS

The Examiner objected to the drawings as not showing every feature of the invention specified in the claims. In particular, the Examiner appears to argue that claim limitations related to "comparing the immediate value and register value" are not shown. Applicants disagree and direct the Examiner's attention to Applicants' specification and figures. Specifically, Figure 3 and 4 describe registers 140 that inherently contain register values (see paragraph [0021], [0027]-[0028] and [0030]). Further, Figure 5 shows an example of an instruction 228 having an immediate value 236 (see paragraph [0026]). If the Examiner is arguing that the process of "comparing an immediate value and register value" is not shown, Applicants have added a method 600 in Figure 6 to address the Examiner's objection. Applicants submit that Figure 6 is not new matter as it is supported by Applicants' specification (*e.g.*, paragraphs [0026]-[0032]) and original claims (*e.g.*, claims 1, 9, 11 and 19).

OBJECTIONS TO THE SPECIFICATION

Applicants hereby update the list of cross-referenced applications with the serial numbers.

OBJECTIONS TO THE CLAIMS

The Examiner argues that claims 1-8 and 19-20 rely on a limitation ("causes the processor to not execute a subsequent instruction") that is not supported in the specification. In response, paragraph [0028] has been amended herewith to address the Examiner's objection. Paragraph [0028] now recites "If the immediate value V does not match the contents of the eight lower bits of the register referenced by Rd, then the instruction that follows the test and skip instruction 228 is 'skipped' or is not executed." The amendment to paragraph [0028] does not add new matter since at least original claims 1 and 19 support the amendment. Further, Applicants' description of skipping a subsequent instruction does not preclude not executing a subsequent instruction.

§ 112 REJECTIONS

The Examiner rejected claims 1-8 and 19-20 under 35 U.S.C. § 112, second paragraph. In the rejection, the Examiner suggests that claim language related to "not executing a subsequent instruction" is unclear or is not supported by the specification. As previously mentioned, paragraph [0028] has been amended based on, at least, original claims 1 and 19 to recite "the instruction that follows the test and skip instruction 228 is 'skipped' or is not executed." For at least this reason, Applicants submit the rejection under 35 U.S.C. § 112, second paragraph should be withdrawn.

§ 102 AND § 103 REJECTIONS

Amended claim 1, in part, requires a "processor [that] executes a test and skip instruction that includes an immediate value and a reference to a register, performs a comparison using the immediate value and the register value stored in the referenced register, and selectively skips a subsequent instruction that follows the test and skip instruction based on the comparison." Terada does not teach "a test and skip instruction" as set forth in claim 1. Instead, Terada teaches a comparison instruction that is separate from a skip instruction. Specifically, Terada's comparison instruction is executed at line 001, then a subtraction instruction is executed at line 002 (see Figure 4). The subtraction instruction includes a predicate register selection field that checks the value of a predicate register "p0". If p0 is false, the subtraction instruction is not executed.

Further, Terada does not disclose whether the instruction actually includes the immediate value. Terada simply mentions that data register region (r1) and immediate value "2" are compared (see col. 6, lines 4-6). The inclusion of an immediate value in an instruction is not inherent as pointed out in Applicants' specification (see paragraph [0030]). For at least these reasons, claim 1 and its dependent claims are allowable over the cited references.

Claim 9 was amended to correct a typographical error and thus the scope of claim 9 has not been affected. Claim 9, in part, requires "if said control bit is in a first state, comparing the immediate value to the contents of the register referenced in the instruction and skipping a subsequent instruction based on the outcome of the comparison" or "if said control bit is in a second state, masking the contents of the register with the immediate value, testing one or more bits in the masked version of the contents of the register, and skipping a subsequent instruction based on the outcome of the testing."

The Examiner recognizes that Terada and Blaner fail to teach an instruction with a control bit that specifies a first or second state, but argues the limitation is obvious. Specifically, the Examiner reasons an instruction with a control bit would have been obvious because "an instruction with two different modes of operation using a control bit is essentially the same as having two different instructions using two separate opcodes" (see Office action dated 02/23/06, page 17). Applicants disagree for several reasons. First, Applicants' instruction (with the control bit) can be decoded and performed in a single cycle by one processor. This is not the case for two different instructions that use two separate opcodes. Second, storing an instruction with a control bit requires less memory space than storing two different instructions that use two separate opcodes. Third, decoding an instruction with a control bit requires some planning as to which bit is the control bit and the significance of the control bit. Two different instructions that use two separate opcodes do not suggest how to implement and interpret an instruction with a control bit that specifies a first or second state.

Further, Blaner's masking is not based on an immediate value provided with an instruction as set forth in claim 9. None of the references cited by the Examiner,

considered individually or together, teach or suggest Applicants' claimed "masking the contents of the register with the immediate value, testing one or more bits in the masked version of the contents of the register, and skipping a subsequent instruction based on the outcome of the testing". For at least these reasons, claim 9 and its dependent claim are allowable over the cited references.

With respect to claim 11, none of the references cited by the Examiner, considered individually or together, teach or suggest a "co-processor [that] selectively operates in a stack-based instruction mode and a register-based instruction mode". Further, claim 11 requires "during the register-based instruction mode, the co-processor executes an instruction that includes an immediate value and a reference to a register accessible to said co-processor, performs a comparison using the immediate value and the register value, and executes or skips a subsequent instruction based on the comparison."

The references cited by the Examiner, considered individually or together, fail to teach or suggest Applicants' claimed "co-processor [that] selectively operates in a stack-based instruction mode and a register-based instruction mode". Terada and Blaner fail to even mention "stacks". Chen mentions "stacks", but fails to teach or suggest a "co-processor [that] selectively operates in a stack-based instruction mode and a register-based instruction mode" as set forth in claim 11. For at least this reason, claim 11 and its dependent claims are allowable over the cited references.

Claim 19, in part, requires "a means for decoding an instruction that includes an immediate value and a reference to a register for performing a comparison using the immediate value and a register value stored in the referenced register, and for causing the processor to execute or not execute a subsequent instruction that follows the instruction based on the comparison." As previously mentioned, Terada does not disclose whether the instruction actually includes the immediate value and the inclusion of an immediate value in an instruction is not inherent. For at least these reasons, claim 19 and its dependent claim are allowable over the cited references.

CONCLUSIONS

Applicants respectfully request reconsideration and that a timely Notice of Allowance be issued in this case. Applicants hereby petition for any time extensions that are necessary to prevent this case from being abandoned. In the event that additional fees related to this Amendment, or other transactions in this case, are required (including fees for net addition of claims and for time extension), the Examiner is authorized to charge Texas Instruments Inc.'s Deposit Account No. 20-0668 for such fees.

Respectfully submitted,

Alan D. Christenson
PTO Reg. No. 54,036
CONLEY ROSE, P.C.
(713) 238-8000 (Phone)
(713) 238-8008 (Fax)
AGENT FOR APPLICANTS